**Group Name: Binary Cartel**

**Project Title: Health Monitoring System**

**Week 6: Instruction Set Architecture and Documentation**

**Course: CS3520**

**Date: 19/10/25**

Overview and Motivation

Processor Context and Target Application Domain

The BCHMS-32 (Binary Cartel Health Monitoring System ISA) is an AI-powered, RISC-based microprocessor designed for next-generation mobile health monitoring and predictive wellness devices. It is optimized for continuous, intelligent processing of multi-sensor data such as heart rate, body temperature, motion, and oxygen saturation directly on the device. The BCHMS-32 integrates lightweight machine learning (ML) acceleration for on-device inference, enabling real-time health anomaly detection, adaptive activity recognition, and personalized health insights without relying on constant cloud connectivity.

Building on the principles of Reduced Instruction Set Computing (RISC) and inspired by RISC-V, BCHMS-32 features a streamlined 32-bit instruction set with uniform encoding to simplify decoding and enhance pipelining efficiency. Its microarchitecture combines low-power data processing with AI-oriented extensions for efficient vector and floating-point operations, which are crucial for computing moving averages, filtering noisy data, and running compact neural network models. This makes it ideal for AI-enabled mobile processors embedded in phones, that require both efficiency and intelligence at the edge.

1.1 Supported Instruction Classes

The BCHMS-32 supports the following instruction classes:

- Arithmetic Instructions: Integer operations including addition, subtraction, multiplication, division, and immediate arithmetic.

- Logical Instructions: Bitwise and shift operations for flexible data manipulation.

- Floating-Point Instructions: Precise floating-point arithmetic and type conversions for AI/ML computations.

- Memory Instructions: Fast and efficient data transfers between registers and memory, supporting word and byte granularity.

- Branch and Jump Instructions: Efficient program control for conditional execution, loops, and subroutines.

- Comparison Instructions: Value comparison and flag setting for decision logic and threshold detection.

- System/I-O Instructions: Manage sensor input/output, data streaming, and inter-module communication.

Design Objectives

The BCHMS-32 architecture is guided by the following design objectives:

- Low Power, High Efficiency: Maintain ultra-low power operation suitable for continuous mobile and wearable use.

- AI-Enhanced Real-Time Processing: Support embedded ML inference for health prediction and anomaly detection directly on the device.

- Simplified Hardware Implementation: Preserve a clean datapath and reduced control complexity for compact, scalable deployment.

- Predictable Pipeline Performance: Implement a 5-stage pipeline (Fetch, Decode, Execute, Memory, Writeback) optimized for deterministic timing.

- Scalability and Extensibility: Reserve opcode space and microarchitectural flexibility for future extensions such as deep learning accelerators, wireless connectivity, and secure data handling.

The BCHMS-32 thus bridges the gap between embedded efficiency and AI intelligence, enabling smarter, more responsive, and power-aware health monitoring within next-generation mobile devices.